

# MERR: Improving Security of Persistent Memory Objects via Efficient Memory Exposure Reduction and Randomization

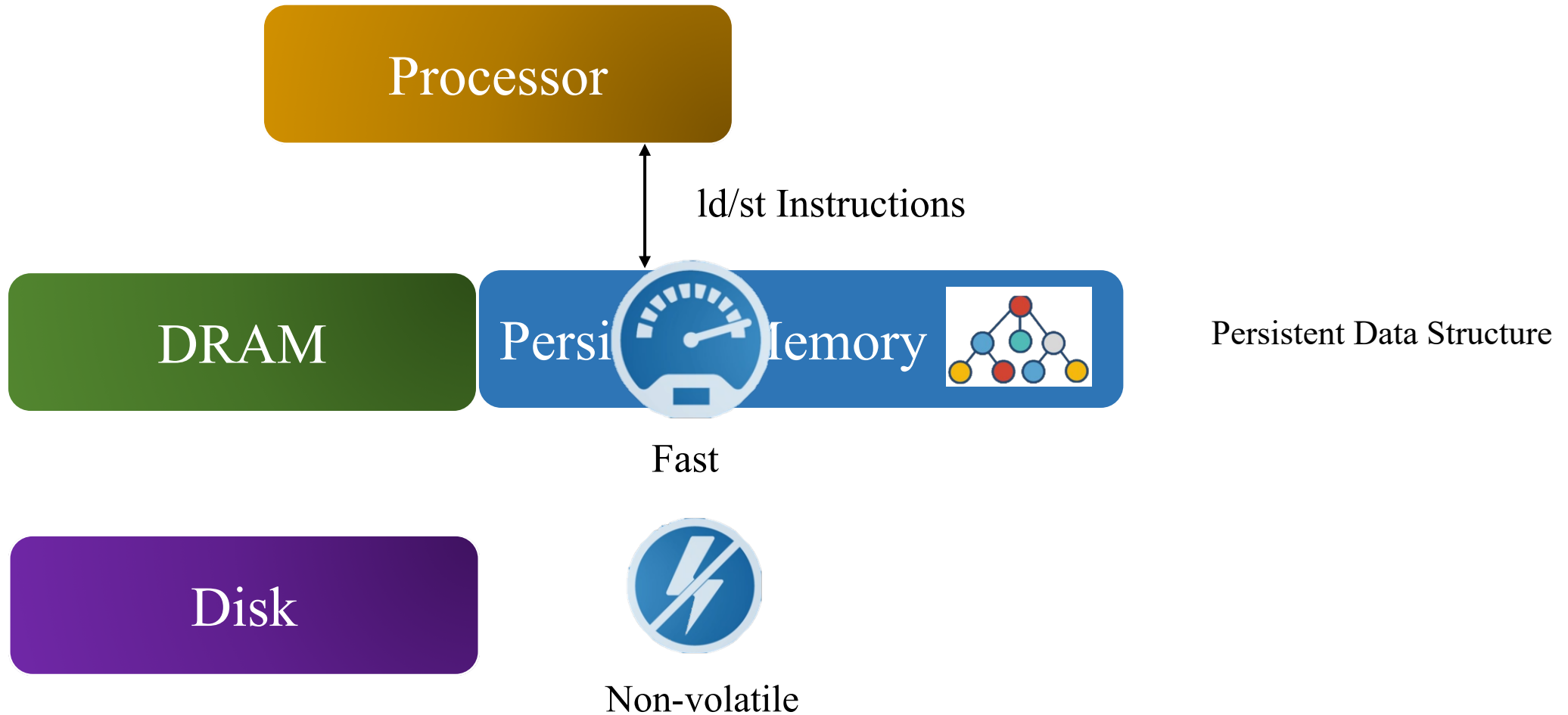
Yuanchao Xu, Yan Solihin, Xipeng Shen

**NC STATE**  
UNIVERSITY



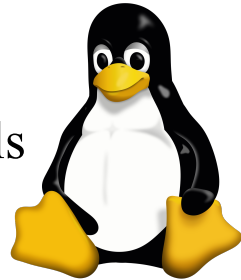
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# Persistent Memory (PM)



# Security is more Important for PM

No System calls



Dangling Pointer

Victim Data

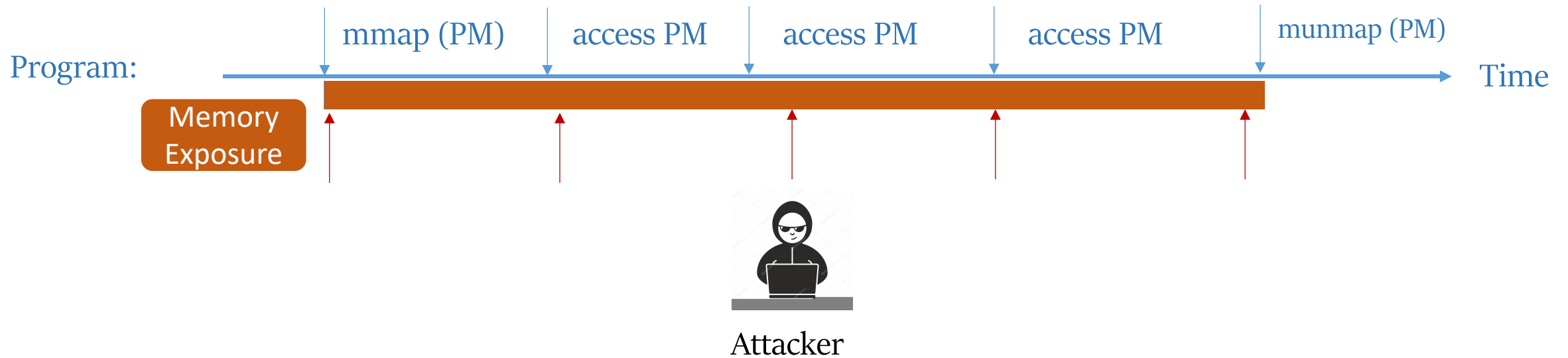


Attacker

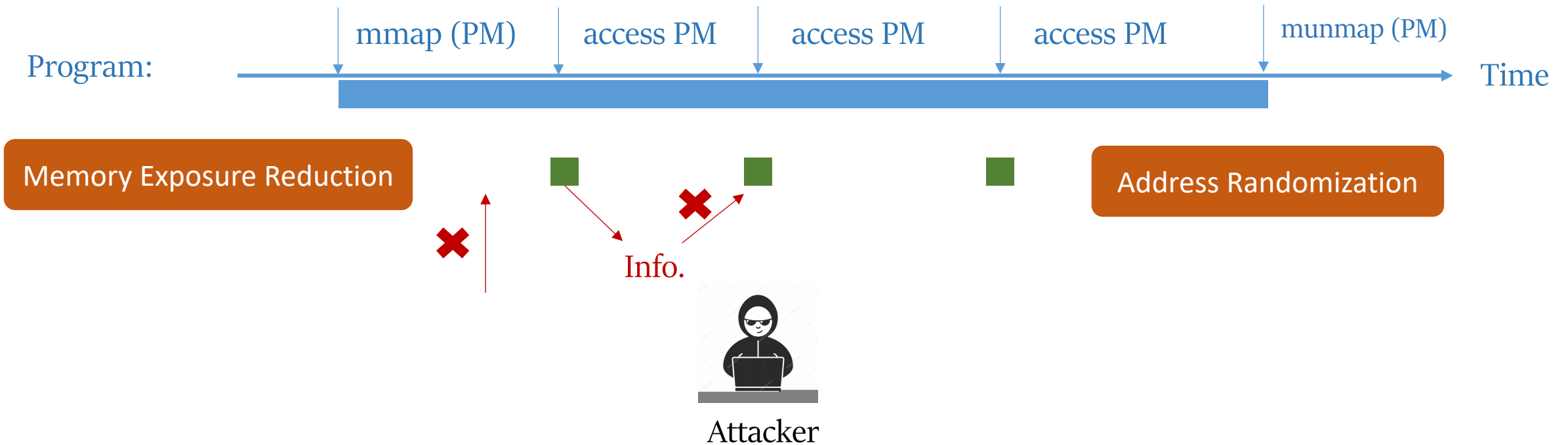


Users

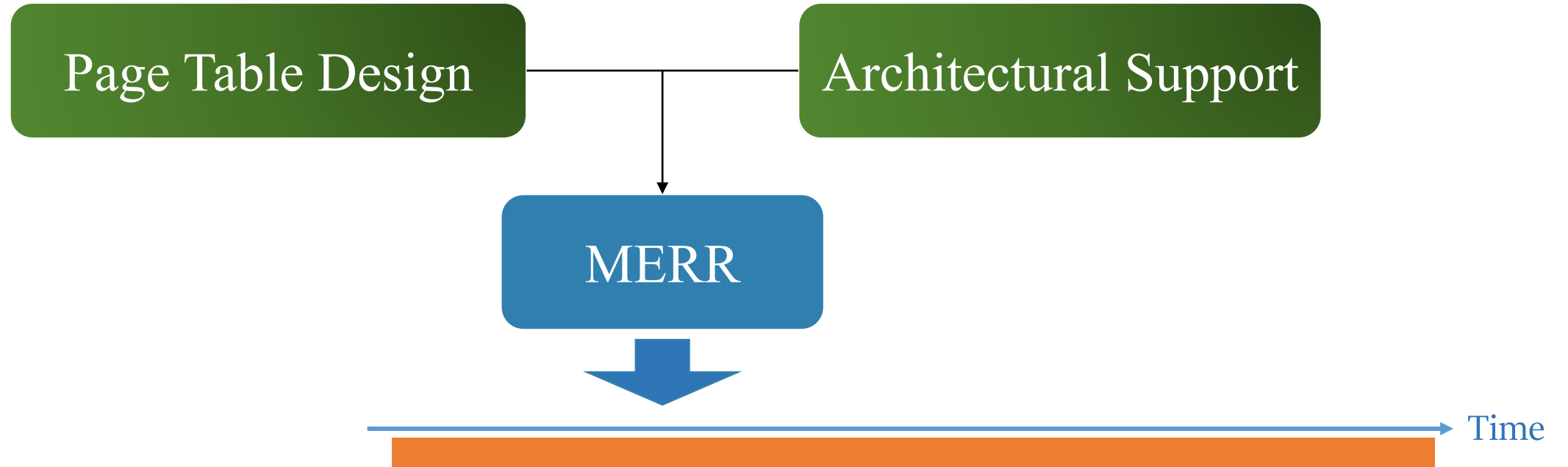
# Idea: Memory Exposure Reduction & Randomization



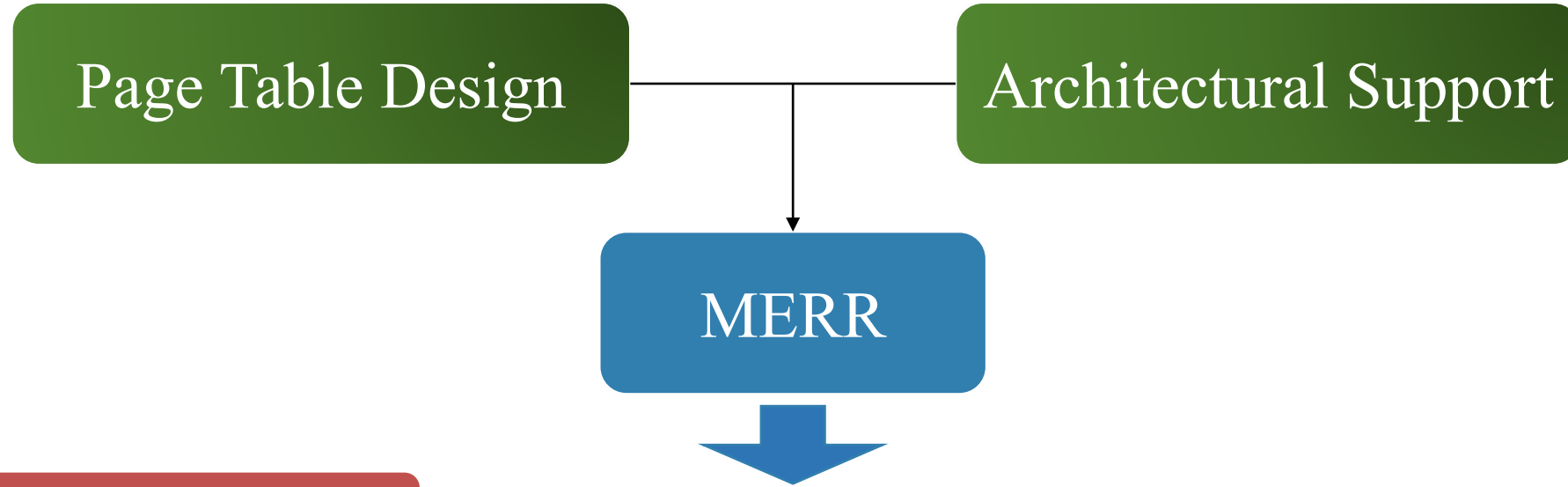
# Idea: Memory Exposure Reduction & Randomization



# MERR



# MERR



70% Reduction 10% Overhead

80us Temporal Window

$10^5$  Randomization Frequency

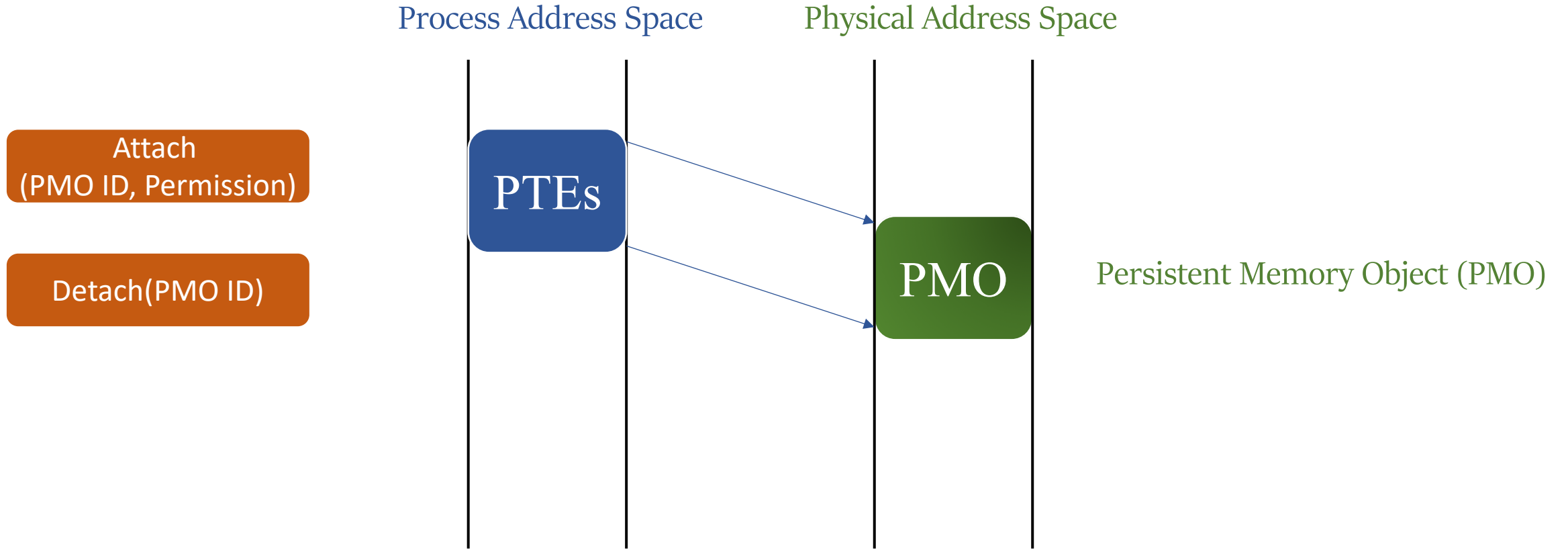


# Outline

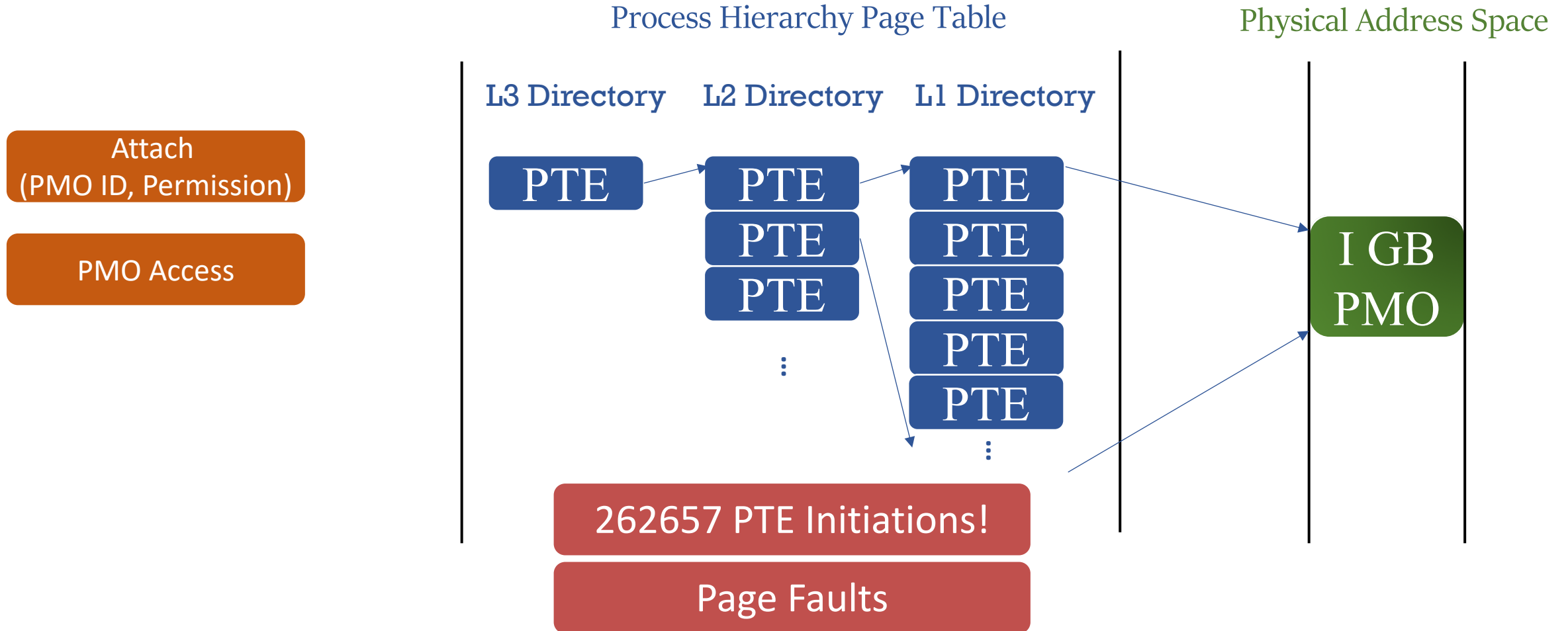
- Attach and Detach system calls
- Page table design
- Randomization
- Architecture support
- Evaluation



# Attach & Detach



# Efficiency Challenge



# Embedding Page Table Subtree

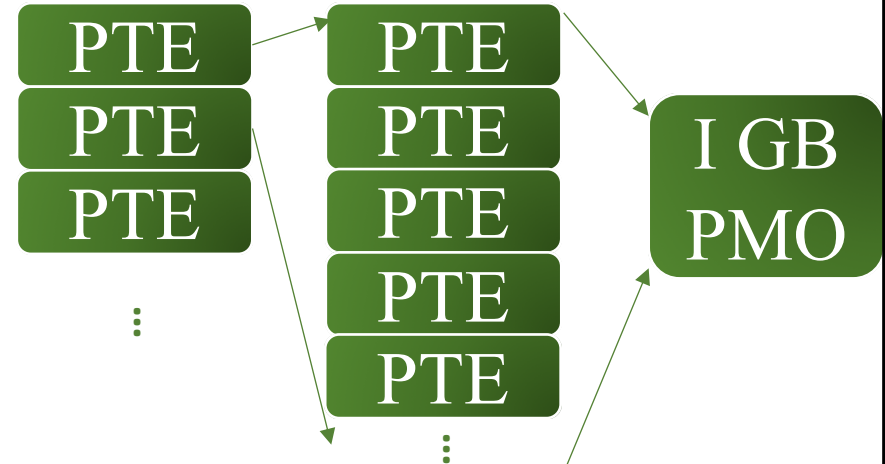
Process Hierarchy Page Table

L3 Directory

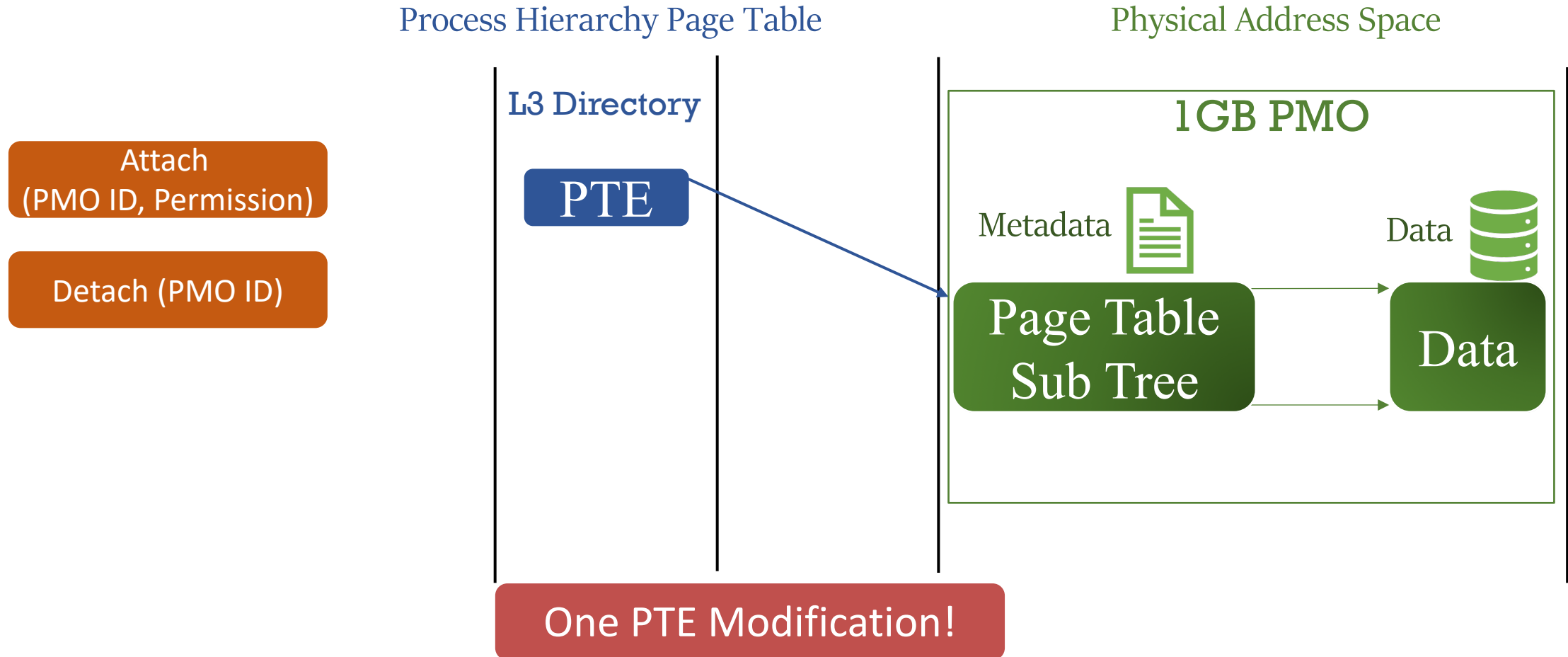
Physical Address Space

L2 Directory

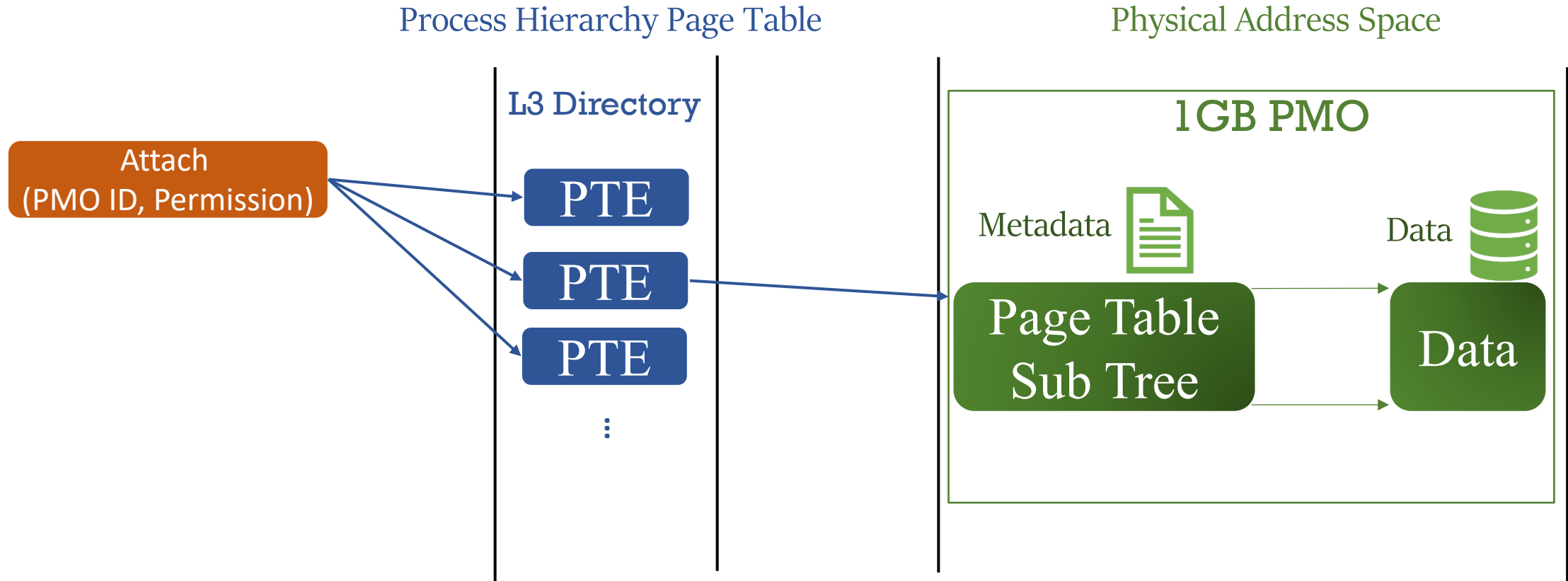
L1 Directory



# Embedding Page Table Subtree



# PMO Space Layout Randomization



# Permission Control Challenges

Process Hierarchy Page Table

Physical Address Space

Attach  
(PMO ID, Permission)

L3 Directory

PTE

1GB PMO

Metadata



Data



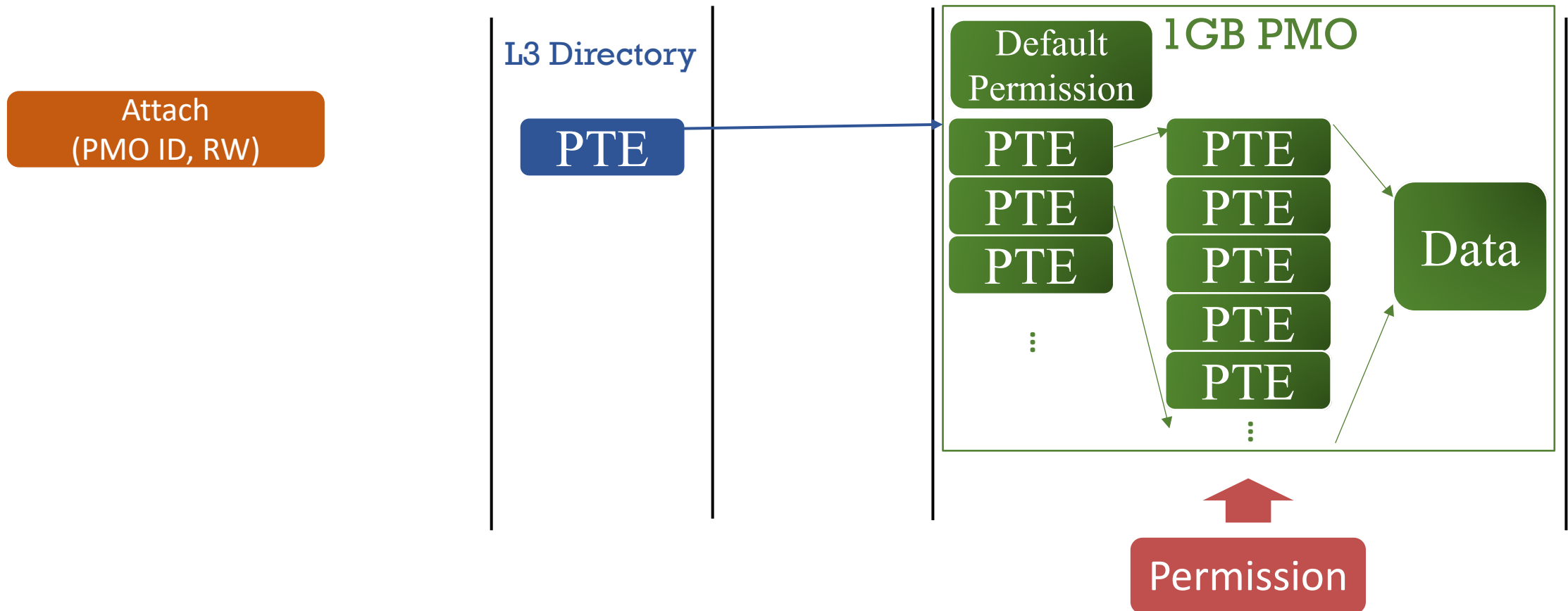
Page Table  
Sub Tree

Data

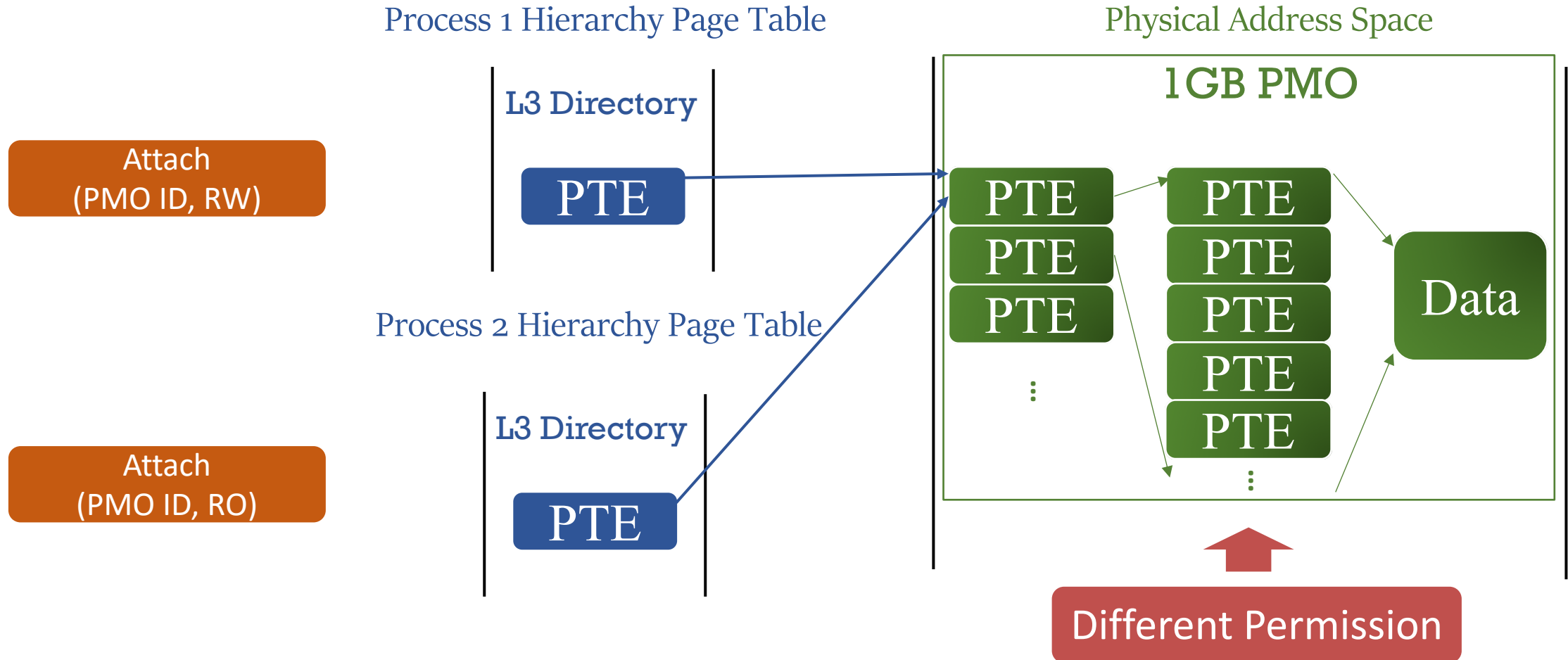
# Permission Control Challenges

Process Hierarchy Page Table

Physical Address Space

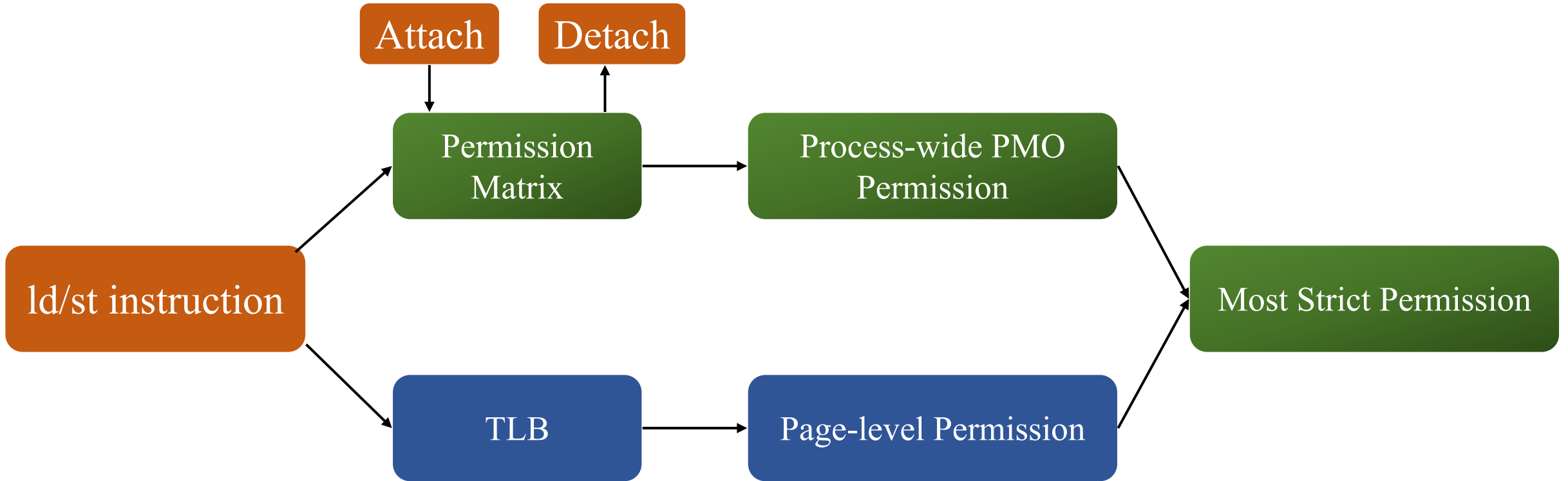


# Permission Control Challenges

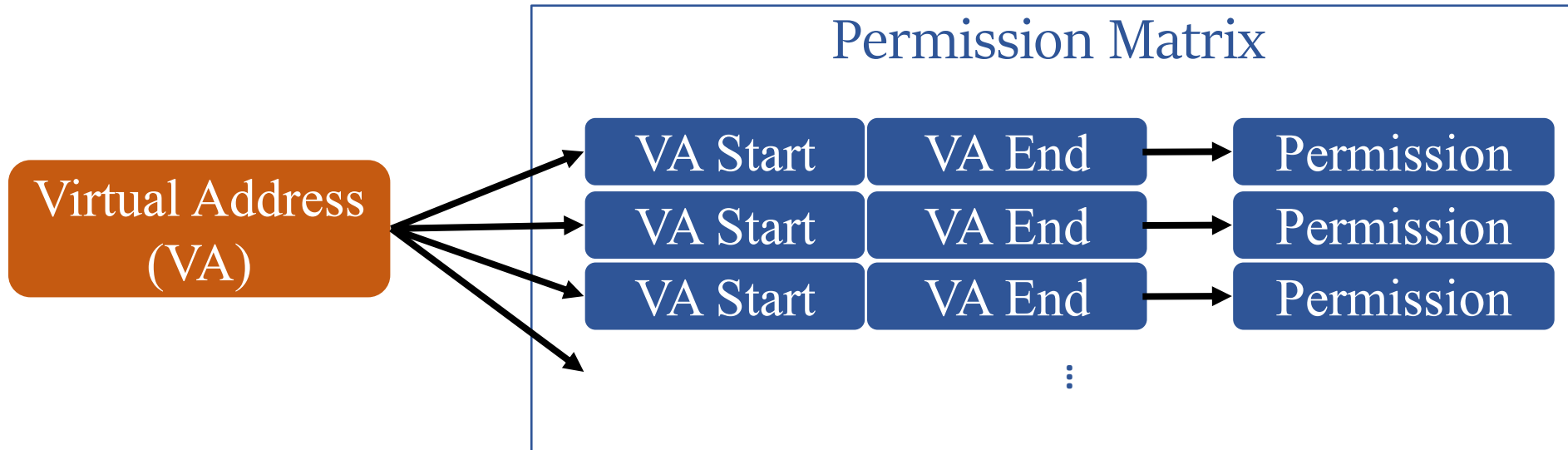




# Permission Matrix

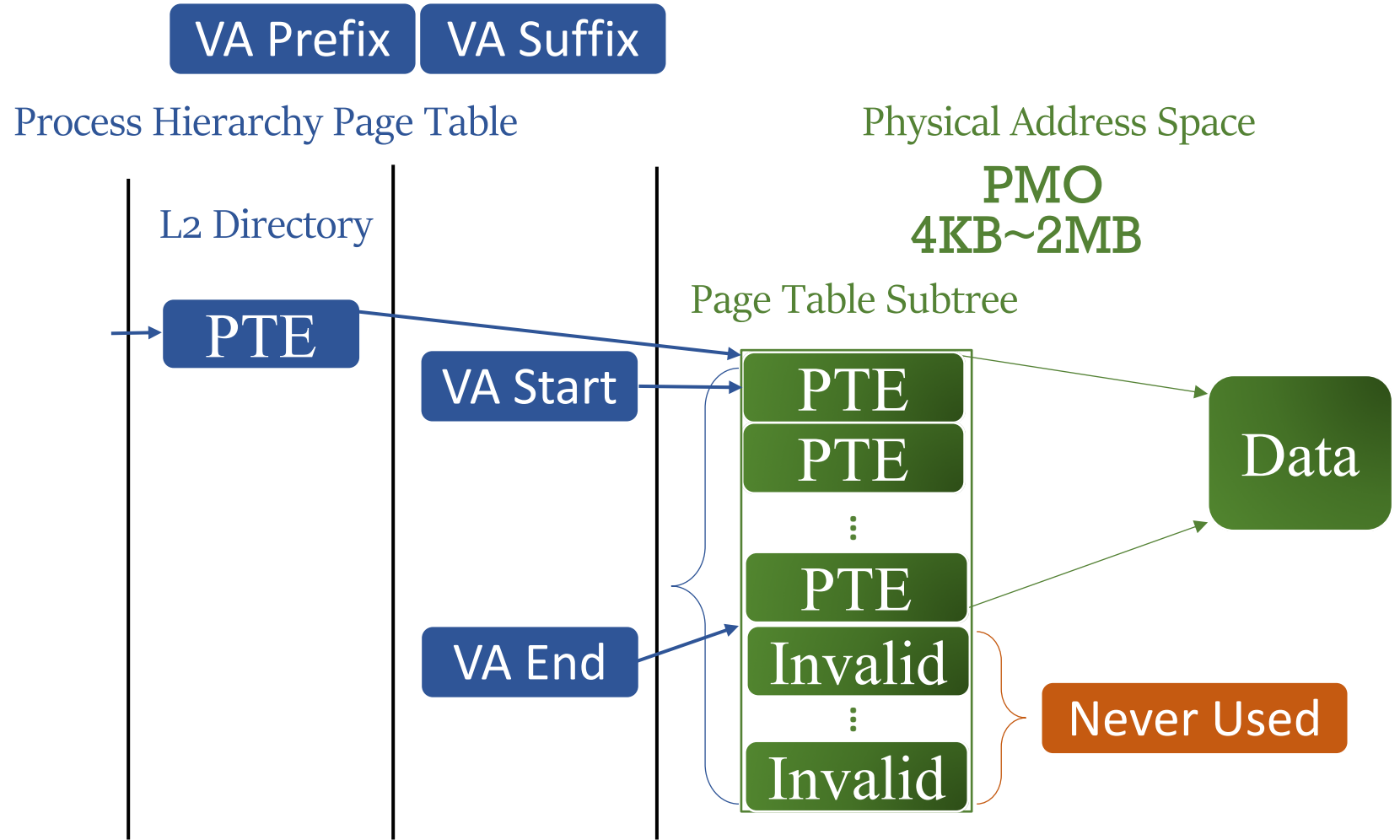


# Permission Matrix Basic Design



High Overhead in Critical Path!

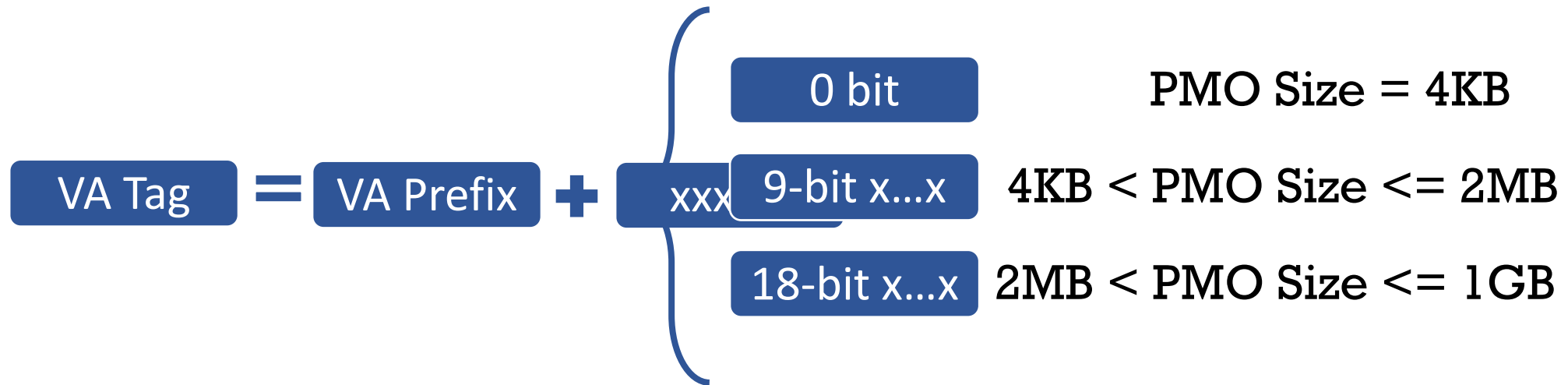
# Virtual Address Tag in Permission Matrix



# Virtual Address Tag in Permission Matrix

$$\text{VA Tag} = \text{VA Prefix} + \text{VA Suffix}$$

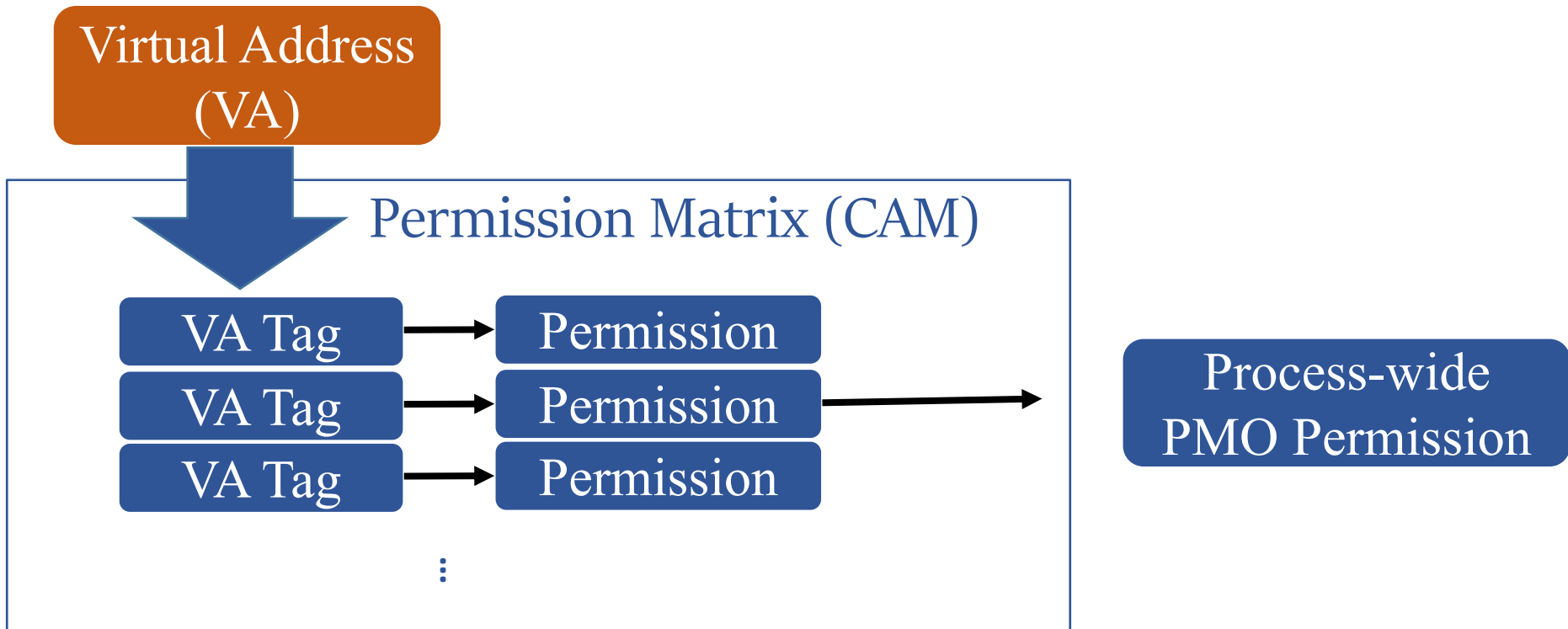
# Virtual Address Tag in Permission Matrix



Content Addressable Memory (CAM) Locate Exact one Entry From VA!

x means all match in Content Addressable Memory

# Permission Matrix Design



# Evaluation Methodology

- Workloads:
  - WHISPER benchmarks
- Operating System Overhead:
  - Implement attach and detach library to replace `mmap()` and `munmap()`
- Architectural Overhead:
  - Intel Pin toolkit
  - Trace-Driven Simulation

# Evaluation Metrics

- Attached Memory Exposure Rate (AMER)

$$\text{AMER} = \frac{\text{Reduced Time}}{\text{Original Time}}$$





# Evaluation Metrics

- Attached Memory Exposure Rate (AMER)
- Memory Exposure Window (MEW)
- PMO Space Layout Randomization Frequency (PSLR Frequency)

$$\text{AMER} = \frac{\text{Reduced Time}}{\text{Original Time}}$$

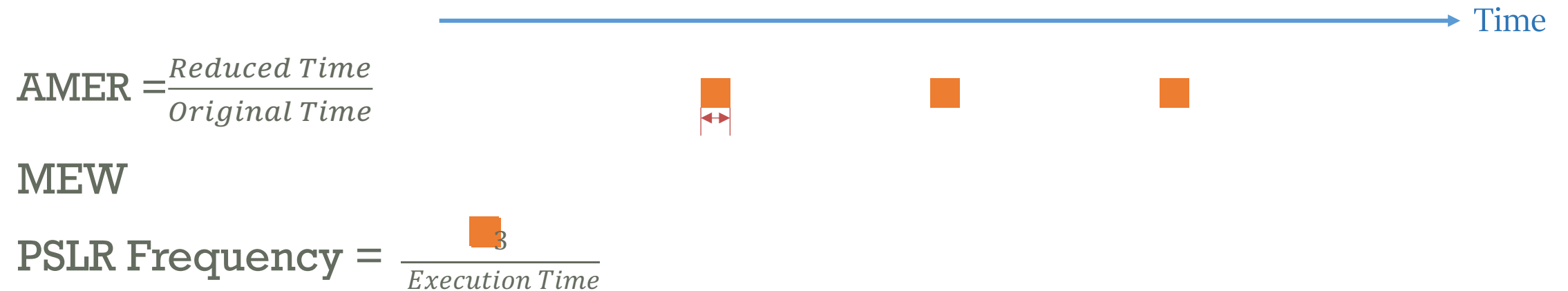


MEW

$$\text{PSLR Frequency} = \frac{\text{Total Times}}{\text{Execution Time}}$$

# Evaluation Metrics

- Attached Memory Exposure Rate (AMER)
- Memory Exposure Window (MEW)
- PMO Space Layout Randomization Frequency (PSLR Frequency)



# Performance

- About 10% overhead

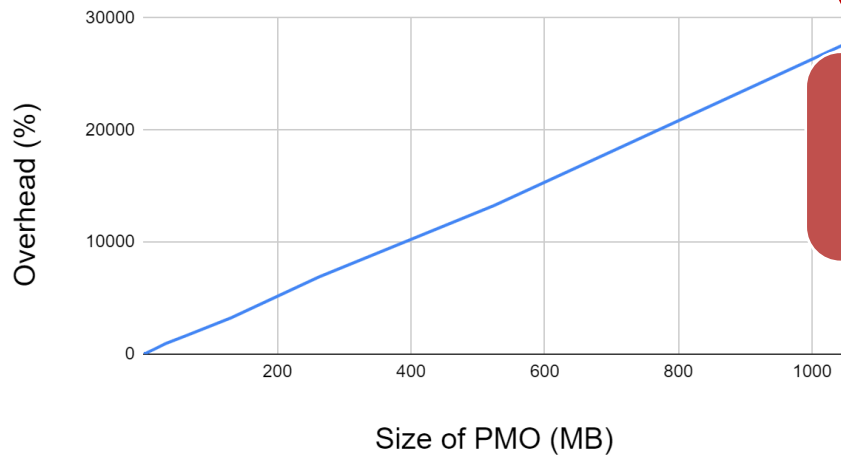
30% AMER (70% Reduction)

80us Maximal MEW

PSLR per 41us

- To achieve above goals

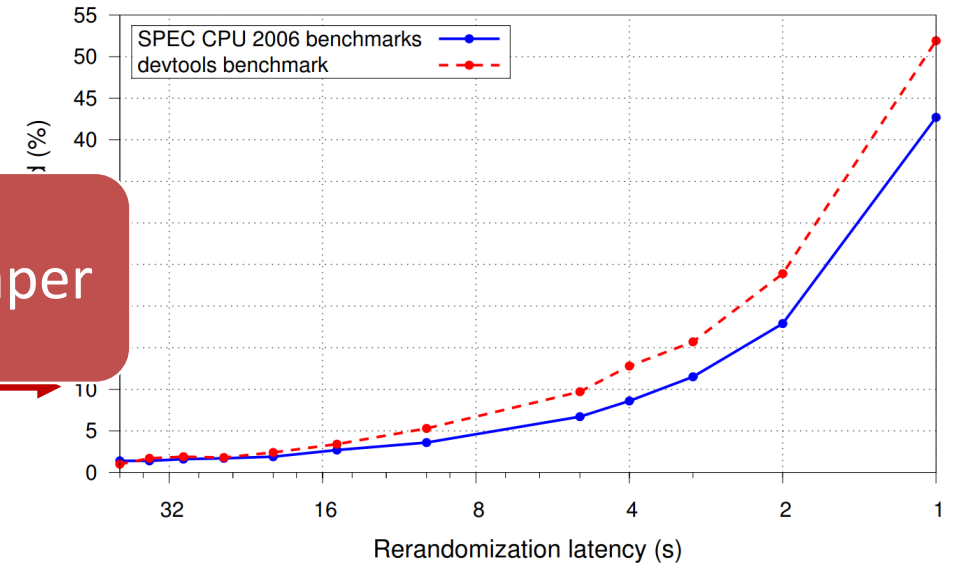
Basic Attach and Detach



2700x Speedup

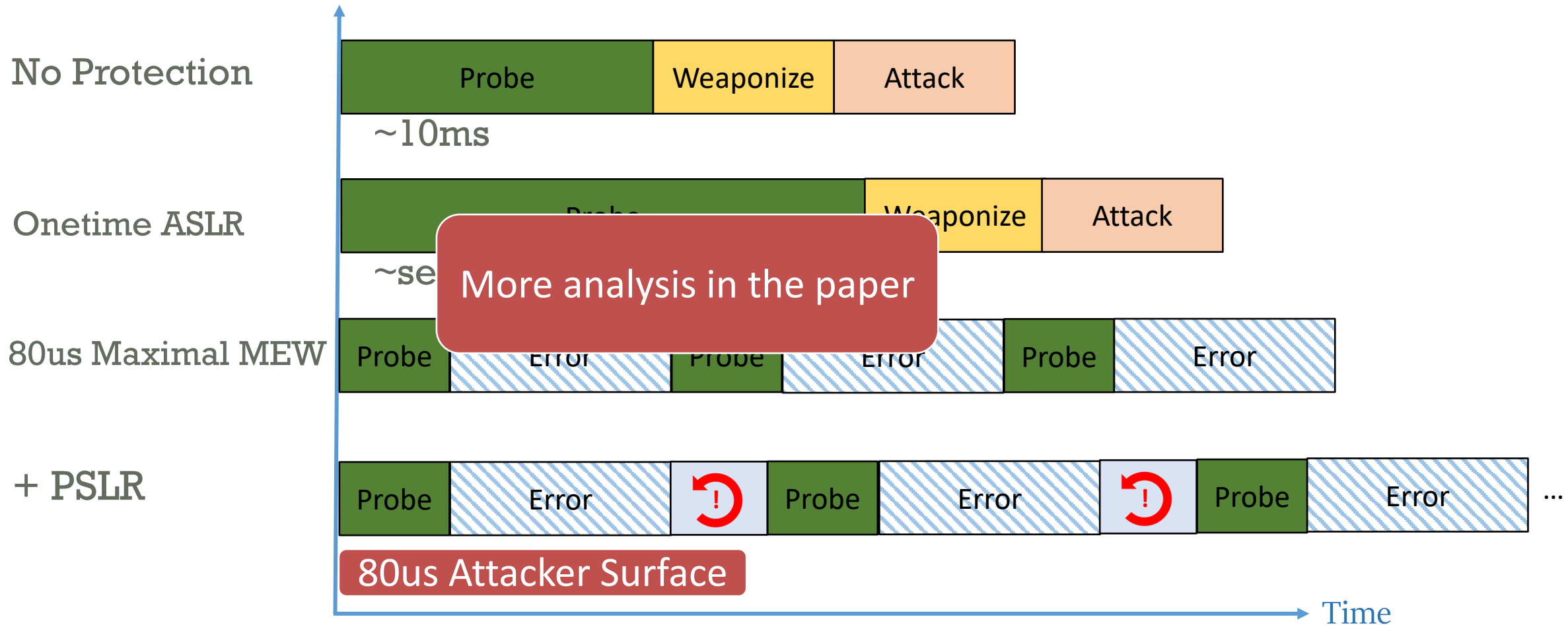
More results in the paper

Enhanced ASLR



$10^5$  per Second Frequency

# Security of MEWR



# Conclusion

- New angle to improve security through **reduce memory exposure and randomization**
- Improved efficiency by **page table design** and **architectural support**
- **Achieved 70% memory exposure reduction** and **80us memory exposure window** with about **10%** overhead on real world applications
- **Provided An Order-of-magnitude** speedup compared to state-of-art runtime randomization